

Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claims 1-22 (cancelled).

Claim 23 (new). A signal level displacement circuit for a flip flop operable to be clocked by a clock signal, the signal level displacement circuit comprising:

a signal delay circuit configured to generate a delayed clock signal corresponding to the clock signal delayed by a time delay;

a circuit node arranged to charge to an operating voltage in a charging phase in response to the clock signal being logically low and to discharge in an evaluation phase depending on a data signal in response to the clock signal being logically high and the delayed clock signal being logically high; and

a capacitor having a programmable capacitance coupling the circuit node to a reference potential.

Claim 24 (new). The signal level displacement circuit as claimed in claim 23, wherein the circuit node is arranged to discharge in the evaluation phase in response to the data signal being logically high and the circuit node is arranged to not discharge in the evaluation phase in response to the data signal being logically low.

Claim 25 (new). The signal level displacement circuit as claimed in claim 23, further comprising:

a first isolating circuit configured to be clocked by the clock signal and having an input connected to the circuit node.

Claim 26 (new). The signal level displacement circuit as claimed in claim 25, further comprising:

a slave latch circuit;

wherein the first isolating circuit has an output connected to the slave latch circuit, the first isolating circuit is configured to generate an output signal at the output, and the slave latch circuit is configured to buffer-store the output signal.

Claim 27 (new). The signal level displacement circuit as claimed in claim 25, further comprising:

a second isolating circuit configured and arranged to be clocked by the delayed clock signal;

wherein an output of the first isolating circuit feeds back to the input of the first isolating circuit via the second isolating circuit.

Claim 28 (new). The signal level displacement circuit as claimed in claim 23, wherein the signal delay circuit, the circuit node, and the capacitor are incorporated into a master latch circuit.

Claim 29 (new). The signal level displacement circuit as claimed in claim 28, wherein:

the master latch circuit further includes an inverter configured to generate and inverted clock signal corresponding to an inversion of the clock signal;

the master latch circuit further includes a first controllable switch driven by the inverted clock signal; and

the first controllable switch switches the operating voltage to the circuit node in response to the clock signal being logically low.

Claim 30 (new). The signal level displacement circuit as claimed in claim 28, wherein:

the master latch circuit further includes a reference potential node configured to be coupled to the reference potential;

the master latch circuit further includes a second, third and fourth controllable switches, the first, second, third, and fourth controllable switches being connected in series with one another between the circuit node and the reference potential node.

Claim 31 (new). The signal level displacement circuit as claimed in claim 30, wherein the master latch circuit is configured to generate a delayed inverted clock signal and to drive the second controllable switch with the delayed inverted clock signal.

Claim 32 (new). The signal level displacement circuit as claimed in claim 30, wherein the third controllable switch is arranged to be driven by the data signal.

Claim 33 (new). The signal level displacement circuit as claimed in claim 30, wherein the fourth controllable switch is arranged to be driven by the clock signal.

Claim 34 (new). The signal level displacement circuit as claimed in claim 30, wherein the capacitor is connected in parallel with the second, third and fourth controllable switches.

Claim 35 (new). The signal level displacement circuit as claimed in claim 28, wherein the time delay is adjustable.

Claim 36 (new). The signal level displacement circuit as claimed in claim 35, wherein during the evaluation phase the capacitor discharges with a time constant in response to the data signal being logically high and the time constant is less than the time delay.

Claim 37 (new). The signal level displacement circuit as claimed in claim 28, wherein the master latch circuit is configured to make the time delay is less than a time period of the clock signal.

Claim 38 (new). The signal level displacement circuit as claimed in claim 28, wherein the signal delay circuit comprises a plurality of inverter stages connected in series.

Claim 39 (new). The signal level displacement circuit as claimed in claim 28, wherein the master latch circuit is configured to receive only a single supply voltage.

Claim 40 (new). A method, comprising:

- using a clocked isolating circuit to isolate a master latch circuit of an edge triggered flip flop from a slave latch circuit of the flip flop; and

- buffer-storing an output signal of the master latch circuit with the slave latch circuit.

Claim 41 (new). A flip flop operable to use a data signal and a clock signal, the flip flop comprising:

- a signal delay circuit configured to generate a delayed clock signal corresponding to the clock signal delayed by a time delay;
- a capacitor configured to generate a programmable capacitance;
- a controllable switch operably coupled between the signal delay circuit and the capacitor; and
- a master latch circuit incorporating at least one of the signal delay circuit, the capacitor, and the controllable switch;

wherein the master latch circuit is configured to charge the capacitor in response to the clock signal being logically low and the master latch circuit is further configured to discharge the capacitor in response to a combination of the clock signal being logically high, the delayed clock signal being logically high, and a state of the data signal.

Claim 42 (new). The flip flop as claimed in claim 24, further comprising:

- a slave latch circuit operably coupled to the master latch circuit;
- wherein the master latch circuit is further configured to generate an output signal on the capacitor and the slave latch circuit is configured to buffer-store the output signal.